

NASA TECH BRIEF

Electronics Research Center



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Saturation Current Spikes Eliminated in Saturable Core Transformers

The problem:

To eliminate the high magnetization current spikes generated by saturable core transformers at the beginning of core saturation. In dc-to-dc power conversion circuits, these high current spikes cause over-

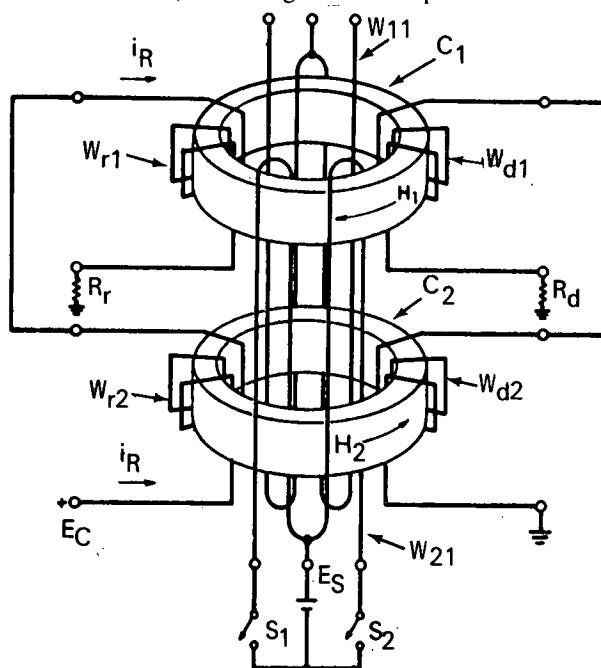


Figure 1.

heating of the power transistors, and destruction eventually occurs.

The solution:

An unsaturating composite magnetic core transformer, consisting of two separate cores in parallel (see Fig. 1), designed so that the impending core saturation causes a signal to be generated, which

is then used to terminate the high current spike in the converter primary circuit.

How it's done:

The transformer comprises two uncut, saturable, magnetic cores C_1 and C_2 , stacked on top of each

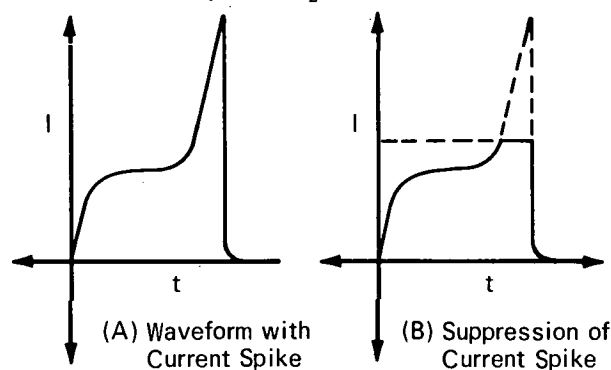


Figure 2.

other. Each core has a pair of control winds W_{r1} and W_{r2} , and sensing windings W_{d1} and W_{d2} connected in series opposition. Both of the cores and their respective control windings are enclosed by common centertapped primary and secondary windings W_{11} and W_{21} , respectively, such that the individual cores operate in parallel within the same transformer core, C_1 . When connected in a conventional dc-to-dc inverter circuit, no signal appears across the resistor R_d as long as the cores are unsaturated, because the control windings have an equal number of turns and have opposite polarity. However, when one of the cores begins to saturate, a voltage E_d developed across R_d activates a switch that removes the input power.

A simplified waveform (see Fig. 2) demonstrates the effectiveness of the transformer in eliminating the

(continued overleaf)

current spikes. The actual circuit implementation for controlling the current flow requires a simple threshold circuit and a sequencing circuit that prevents the continuation of the inverter cycle until S_1 has reopened. This operation virtually eliminates the main cause of power failure and enables the power transistor to process twice the load current than is presently available.

Note:

Requests for further information may be directed to:

Technology Utilization Officer
Headquarters
National Aeronautics
and Space Administration
Washington, D.C. 20546
Reference: TSP71-10142

Patent status:

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